

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

- 5 Claim 1 (currently amended) A method for implementing circuit layouts in a chip, comprising:

forming a plurality of sub-circuit cells with the same layout in different positions of the chip, where each sub-circuit cell comprising at least two types of sub-circuit blocks; and

- 10 when the sub-circuit cells in different positions require different circuit functions, performing a layout programming in at least a connection layer so that different layouts are formed in different positions of the connection layer corresponding to the sub-circuit cells, wherein each layout in the connection layer corresponding to each sub-circuit cell is selectively connected to the
15 sub-circuit blocks of each sub-circuit cell so that the sub-circuit cells in different positions implement different circuit functions.

Claim 2 (original) The method of claim 1, wherein the connection layer is a metal layer.

- 20 Claim 3 (original) The method of claim 1, the layout programming is only performed in the connection layer so that the sub-circuit cells with different circuit functions have different layouts only in the connection layer.

- 25 Claim 4 (cancelled)

Claim 5 (original) The method of claim 1, wherein the sub-circuit cells in different positions are for implementing input/output (I/O) circuits with different I/O functions.

- 30 Claim 6 (original) The method of claim 5, wherein the sub-circuit cells in different positions are for implementing I/O circuits with a Schmidt trigger function.

Claim 7 (original) The method of claim 5, wherein the sub-circuit cells in different positions are for implementing I/O circuits with different slew rates.

- 5 Claim 8 (original) The method of claim 5, wherein the sub-circuit cells in different positions are for implementing I/O circuits with different driving currents.

Claim 9 (currently amended) A chip, comprising:

10 a plurality of layout layers comprising a plurality of same layouts in a plurality of positions of the layout layers so as to implement a plurality of sub-circuit cells with the same layout, each sub-circuit cell comprising at least two types of sub-circuit blocks; and

at least a connection layer comprising different layouts corresponding to the different positions of the layout layers, wherein each layout of the connection layer selectively connects the sub-circuit blocks of each corresponding sub-circuit cell so that the sub-circuit cells in different positions implement different circuit functions.

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Claim 10 (original) The chip of claim 9, wherein the connection layer is a metal layer.

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Claim 11 (cancelled)

Claim 12(original) The chip of claim 9, wherein the connection layer implements input/output (I/O) circuits with different I/O functions by the sub-circuit cells in different positions.

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Claim 13 (original) The chip of claim 12, wherein the connection layer implements I/O circuits with a Schmidt trigger function with the sub-circuit cells in different positions.

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Claim 14 (original) The chip of claim 12, wherein the connection layer implements I/O circuits with different slew rates with the sub-circuit cells in different positions.

Claim 15 (original) The chip of claim 12, wherein the connection layer implements I/O circuits with different driving currents with the sub-circuit cells in different positions.

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